

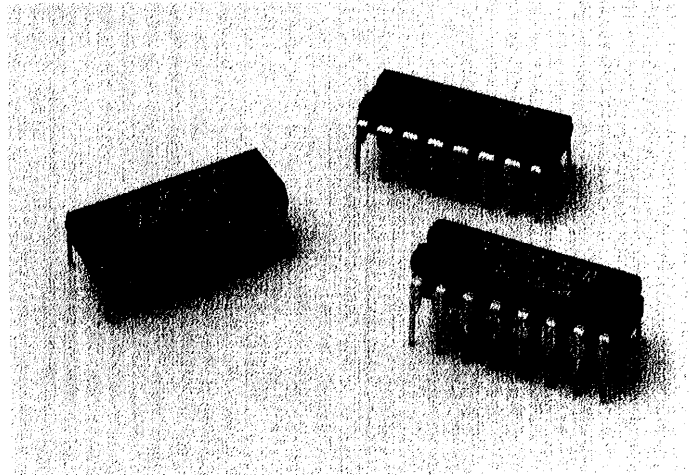
402-990



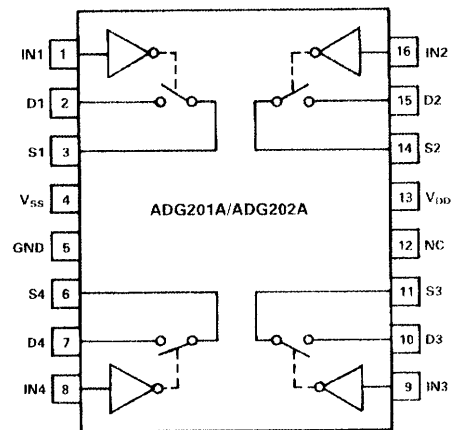
# CMOS Quad SPST Switches

## FEATURES

- 44V Supply Maximum Rating
- ± 15V Analog Signal Range
- Low  $R_{ON}$  (60Ω)
- Low Leakage (0.5nA)
- Low Power Dissipation (33mW)
- TTL/CMOS Compatible
- Superior Second Source:  
ADG201A Replaces DG201A, HI-201  
ADG202A Replaces DG202



## PIN CONFIGURATION (TOP VIEW)



## GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC<sup>2</sup>MOS process which gives an increased signal handling capability of ± 15V. These switches also feature high switching speeds and low  $R_{ON}$ .

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

## PRODUCT HIGHLIGHTS

1. Extended Signal Range:  
These switches are fabricated on an enhanced LC<sup>2</sup>MOS process, resulting in high breakdown and an increased analog signal range of ± 15V.
2. Single Supply Operation:  
For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:  
Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

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Telex: 174059 Cables: ANALOG NORWOODMASS

# SPECIFICATIONS

( $V_{DD} = +15V$ ,  $V_{SS} = -15V$ , unless otherwise noted)

Parameter	ADG201AKN ADG202AKN		ADG201ABQ ADG202ABQ		ADG201ATQ ADG202ATQ		Units	Test Conditions
	25°C	0 to +70°C	25°C	-25°C to +85°C	25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	-10V < $V_S$ < +10V $I_{DS} = 1.0mA$ Test Circuit 1
$R_{ON}$	60		60		60		Ω typ	
	90	145	90	145	90	145	Ω max	
$R_{ON}$ vs. $V_D$ ( $V_S$ )	20		20		20		% typ	$V_S = 0V$ , $I_{DS} = 1mA$
$R_{ON}$ Drift	0.5		0.5		0.5		%/°C typ	
$R_{ON}$ Match	5		5		5		% typ	
$I_S$ (OFF)	0.5		0.5		0.5		nA typ	$V_D = ±14V$ ; $V_S = ∓14V$ ; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
$I_D$ (OFF)	0.5		0.5		0.5		nA typ	$V_D = ±14V$ ; $V_S = ∓14V$ ; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
$I_D$ (ON)	0.5		0.5		0.5		nA typ	$V_D = ±14V$ ; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
<b>DIGITAL CONTROL</b>								
$V_{INH}$ High Threshold		2.4		2.4		2.4	V min	
$V_{INL}$ Low Threshold		0.8		0.8		0.8	V max	
$I_{INL}$ or $I_{INH}$		1		1		1	μA max	
<b>DYNAMIC CHARACTERISTICS</b>								
$t_{OPEN}$	30		30		30		ns typ	Test Circuit 4
$t_{ON}^1$	300		300		300		ns max	
$t_{OFF}^1$	250		250		250		ns max	
OFF Isolation	80		80		80		dB typ	$V_S = 10V(p-p)$ ; $f = 100kHz$ $R_L = 75Ω$ ; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	
$C_S$ (OFF)	5		5		5		pF typ	Test Circuit 7
$C_D$ (OFF)	5		5		5		pF typ	
$C_{DS}$ (ON)	16		16		16		pF typ	$R_S = 0Ω$ ; $C_L = 1000pF$ ; $V_S = 0V$ Test Circuit 5
$C_{IN}$ Digital Input Capacitance	5		5		5		pF typ	
$Q_{INJ}$ Charge Injection	20		20		20		pC typ	
<b>POWER SUPPLY</b>								
$I_{DD}$	0.6		0.6		0.6		mA typ	Digital Inputs = $V_{INL}$ or $V_{INH}$
$I_{DD}$		2		2		2	mA max	
$I_{SS}$	0.1		0.1		0.1		mA typ	
$I_{SS}$		0.2		0.2		0.2	mA max	
Power Dissipation		33		33		33	mW max	

## NOTES

<sup>1</sup>Sample tested at 25°C to ensure compliance.

Specifications subject to change without notice.

### ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C unless otherwise stated)

V <sub>DD</sub> to V <sub>SS</sub> . . . . .	44V
V <sub>DD</sub> to GND . . . . .	25V
V <sub>SS</sub> to GND . . . . .	-25V
<b>Analog Inputs<sup>1</sup></b>	
Voltage at S, D . . . . .	V <sub>SS</sub> to V <sub>DD</sub>
Continuous Current, S or D . . . . .	30mA
Pulsed Current S or D	
I <sub>ms</sub> Duration, 10% Duty Cycle . . . . .	70mA
<b>Digital Inputs<sup>1</sup></b>	
Voltage at IN . . . . .	V <sub>SS</sub> - 2V to V <sub>DD</sub> + 2V or 20mA, Whichever Occurs First

### Power Dissipation (Package)

<b>Plastic DIP</b>	
Up to +75°C . . . . .	470mW
<b>Cerdip</b>	
Up to +75°C . . . . .	900mW/°C
Derates above +75°C by . . . . .	12mW/°C

### Operating Temperature

Plastic (KN Version) . . . . .	0 to +70°C
Cerdip (BQ Version) . . . . .	-25°C to +85°C
Cerdip (TQ Version) . . . . .	-55°C to +125°C
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . .	+300°C

### NOTE

<sup>1</sup>Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



### ADG201A/ADG202A FUNCTIONAL DIAGRAM

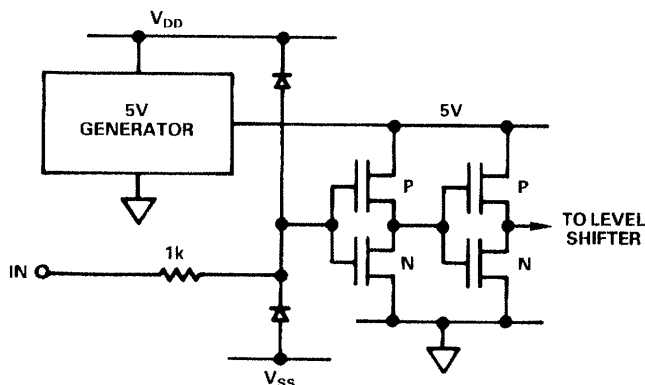
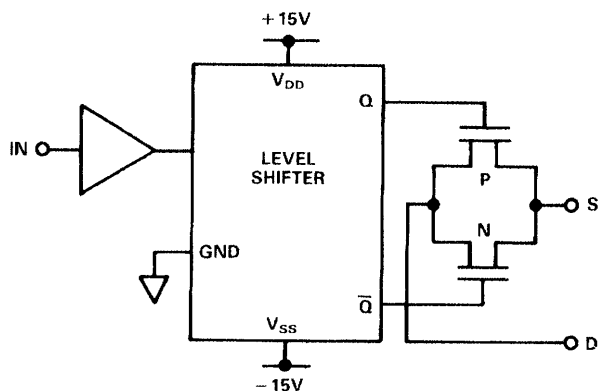


Figure 1. Typical Digital Input Cell

### ORDERING INFORMATION<sup>1,2</sup>

Plastic 0 to +70°C	Cerdip <sup>3</sup> -25°C to +85°C	Cerdip <sup>3</sup> -55°C to +125°C
ADG201AKN	ADG201ABQ	ADG201ATQ
ADG202AKN	ADG202ABQ	ADG202ATQ

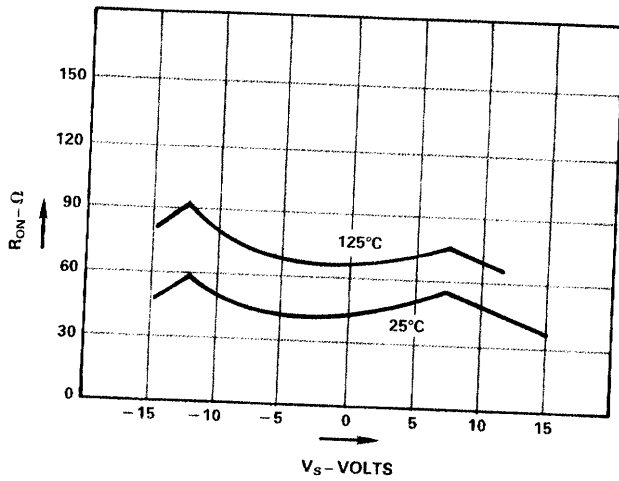
### NOTES

<sup>1</sup>To order military standard 883B REV C processed parts, add /883B to part number. Contact your local sales office for military data sheet.

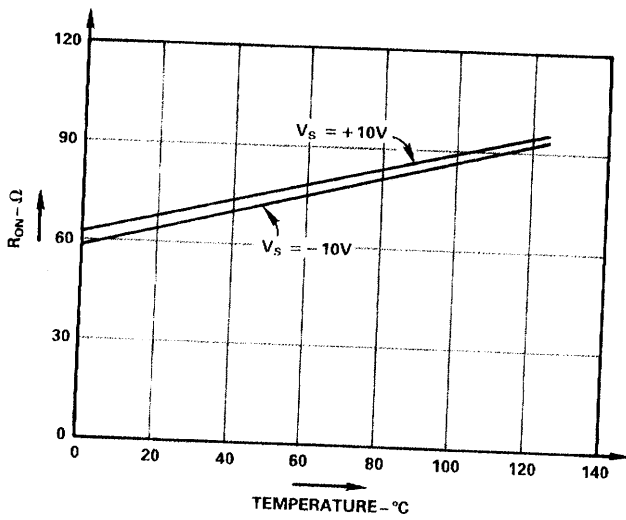
<sup>2</sup>Leadless Ceramic Chip Carrier versions are available. To order, replace Q with E. Plastic Leaded Chip Carrier versions are also available. To order, replace N with P.

<sup>3</sup>Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

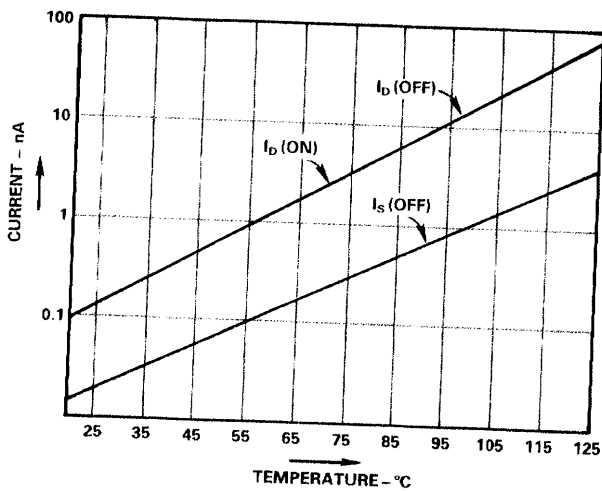
# Typical Performance Characteristics



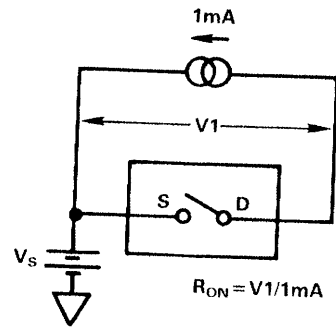
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ )



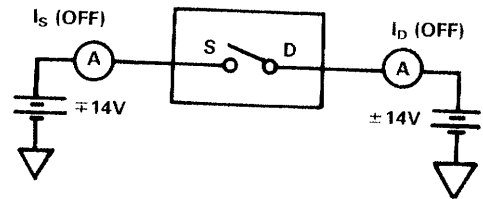
$R_{ON}$  as a Function of Temperature



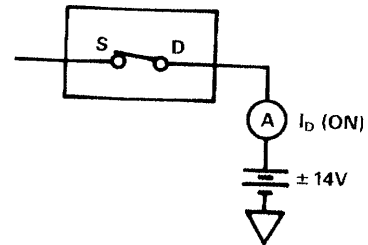
Leakage Current as a Function of Temperature



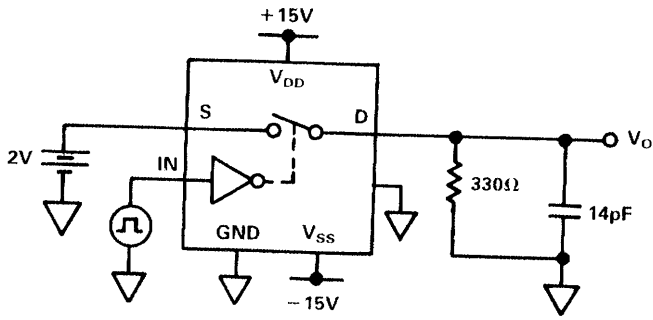
Test Circuit 1



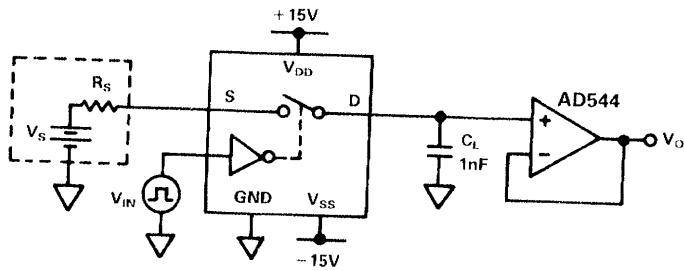
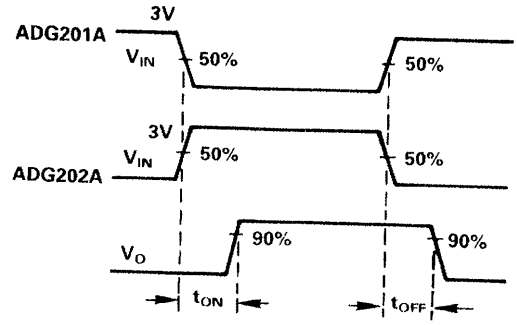
Test Circuit 2



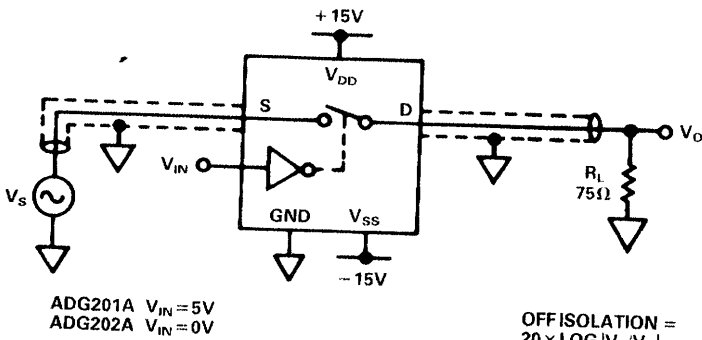
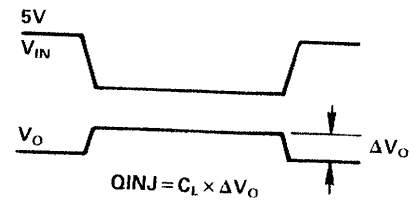
Test Circuit 3



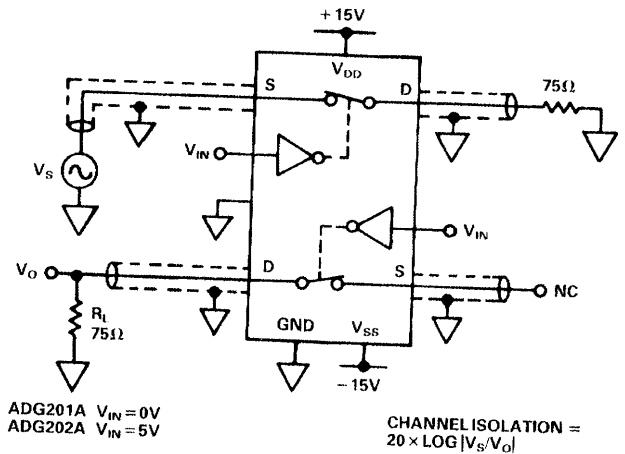
Test Circuit 4



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation



Test Circuit 7. Channel to Channel Isolation

## TERMINOLOGY

$R_{ON}$	Ohmic resistance between terminals OUT and S
$R_{ON}$ Match	Difference between the $R_{ON}$ of any two channels
$I_S$ (OFF)	Source terminal leakage current when the switch is off
$I_D$ (OFF)	OUT terminal leakage current when the switch is off
$I_D$ (ON)	Leakage current that flows from the closed switch into the body
$V_D$ (V <sub>S</sub> )	Analog voltage on terminal D, S
$C_S$ (OFF)	Switch input capacitance "OFF" condition
$C_D$ (OFF)	Switch output capacitance "OFF" condition
$C_{IN}$	Digital input capacitance
$C_{DS}$ (ON)	Input to output capacitance when the switch is on

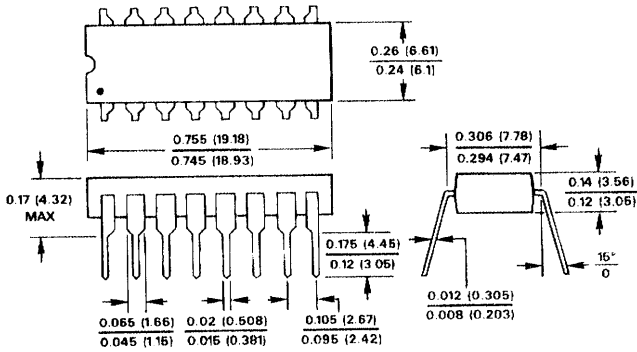
$t_{ON}$	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
$t_{OFF}$	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
$t_{OPEN}$	"OFF" time measured between 50% points of both switches when switching from one address state to another
$V_{INL}$	Threshold voltage for low state
$V_{INH}$	Threshold voltage for high state
$I_{INL}$ ( $I_{INH}$ )	Input current of the digital input
$V_{DD}$	Most positive voltage supply
$V_{SS}$	Most negative voltage supply
$I_{DD}$	Positive supply current
$I_{SS}$	Negative supply current

## MECHANICAL INFORMATION

### OUTLINE DIMENSIONS

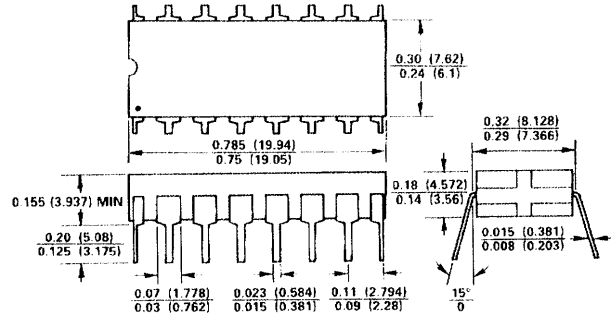
Dimensions shown in inches and (mm).

#### 16-PIN PLASTIC (SUFFIX N)

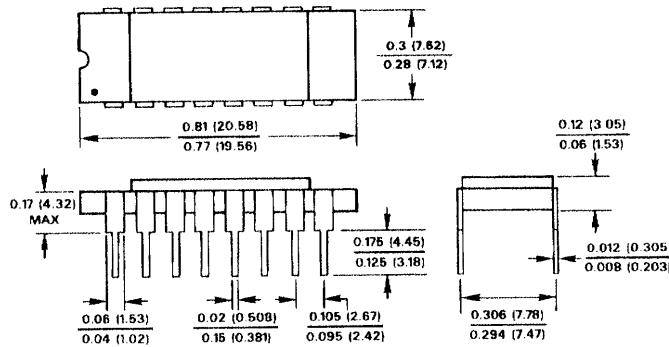


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

#### 16-PIN CERDIP (SUFFIX Q)



#### 16-PIN CERAMIC DIP<sup>1</sup>



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH  
LEADS WILL BE EITHER GOLD OR TIN PLATED  
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

NOTE  
<sup>1</sup>ANALOG DEVICES RESERVES THE RIGHT TO  
SHIP CERAMIC PACKAGES IN LIEU OF CERDIP  
PACKAGES.